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Microelectronics, Nanoelectronics, and the Future of Electronics

Jing Wang
Mark Lundstrom
Purdue University

4.1 Introduction

Silicon technology continues to progress rapidly, with current generation technologies having physical gate lengths well below 100 nm. At the same time, remarkable advances in nonsilicon nano- and molecular technologies are occurring. It is time to think seriously about the role that nanoelectronics and nontraditional technologies could play in future electronic systems. Moore's law describes device scaling-down in integrated circuits, which has led an unprecedented growth of the semiconductor industry. At the same time, it also carried device researchers into the nano world. Well-established concepts from mesoscopic physics [1] are now entering the working knowledge of device physicists and engineers as silicon transistors enter the nanoscale [2]. At the micrometer scale, transistors were well described by drift-diffusion equations, but now people are beginning to use a new language to describe nanoscale transistors. In addition, several interesting new devices that may have important applications are also being developed [3–6].

Nanoelectronics can play an important role in future electronic systems, if the design community is engaged to exploit the opportunities that nanoelectronics offers. Therefore, we appreciate this opportunity to give an overview of the current developments of nanoscale transistors. The chapter begins by defining nanotechnology and discussing how a metal-oxide-semiconductor field-effect transistor (MOSFET) performs in the nanometer regime (Section 4.2), then examines the ultimate scaling limit and

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practical limits of the silicon MOSFET (Section 4.3 and Section 4.4). After that, several new types of field-effect transistors (FETs) are introduced, which may become the substitutes for the silicon MOSFET (Section 4.5) and other nanotransistors beyond the FET (Section 4.6). Several important issues in the research of nanoelectronics are also discussed (Section 4.7). To be concise, we do not include the detailed mathematical formalism of the device theory, but the references are listed to help the reader who has particular interests find the sources.

4.2 The Silicon MOSFET as a Nanoelectronic Device

4.2.1 What Is Nanotechnology?

Nanotechnology has been defined as work at the 1–100-nm length scale to produce structures, devices, and systems that have novel properties because of their nanoscale dimensions [7]. Some insist that two dimensions lie in the 1–100 nm regime, which would rule out traditional technologies such as thin films. A key part of the definition is that new phenomena occur (caused, for example, by the dominance of interfaces and quantum mechanical effects), and that these new phenomena may be exploited to improve the performance of materials, devices, and systems. Nanotechnologies also involve the manipulation and control of matter at the nanoscale. Semiconductor technology does much of this with a "top-down" approach that lithographically imposes a pattern, and then etches away bulk material to create a nanostructure. Some argue that self-assembly is an essential component of nanotechnology. The hope is that nanostructures can be self-assembled from the "bottom up," molecule by molecule. We argue that current-day silicon technology meets the definition of nanoelectronics, that future silicon technologies will meet it even better, and that nontraditional technologies could play an important role in future electronic systems by complementing the capabilities of nanoscale silicon technology, rather than by attempting to replace it.

4.2.2 Silicon MOSFETs in the Nanometer Regime

The International Technology Roadmap for Semiconductors (ITRS) [8] calls for 9-nm physical gate lengths for integrated circuit (IC) transistors in 2016. At the same time, major IC manufacturers have reported transistors with 10-nm (or shorter) gate lengths on IEDM 2002 [9,10], which demonstrate the promise of pushing IC technology to the 10-nm regime.

To scale silicon transistors down to the 10-nm scale, new device structures are needed to suppress the short channel effects [11]. Figure 4.1 is a schematic illustration of a fully depleted, double-gate (DG) MOSFET, a device that offers good prospects for scaling silicon transistors to their limits [12]. Other approaches (e.g., the FinFET [9] and the tri-gate MOSFET [13]) are also being explored. At a 9-nm gate length, acceptable short-channel effects require a fully depleted silicon body thickness of 3 nm or less, and an equivalent gate oxide thickness of less than 1 nm. At such dimensions, the properties of the silicon material will be affected by quantum confinement (e.g., the bandgap will increase), and device properties will be influenced by quantum transport.

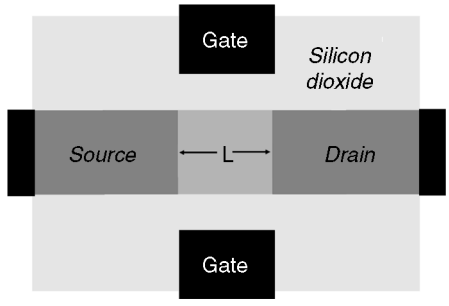

FIGURE 4.1 The double-gate MOSFET structure.

Traditional device equations are based on the drift-diffusion theory [11], which assumes that the device scale is much larger than the electron wavelength (~ 8nm at room temperature) and the electron mean-free-path (the average distance an electron travels between two collisions, ~ 10nm for electrons in the inversion layer). The first assumption allows us to treat electrons as classical particles with zero size, and the second one justifies the "local transport" property (the electron velocity at a position is solely determined by the local electric field and mobility). Unfortunately, at the nanoscale, neither of these assumptions is well satisfied. As a result, to capture the new physical effects that occur at the nanoscale, the old device theory must be modified or even completely replaced by a new quantum transport theory.

Four important phenomena need to be properly treated in the modeling of nanotransistors:

1. Quantum confinement
2. Gate tunneling
3. Quasi-ballistic transport
4. Source-to-drain (S/D) tunneling

The first two effects occur in the confinement direction (normal to the gate electrode(s)) of the MOSFET. As silicon technology entered the sub-100-nm regime (the corresponding oxide thickness < 3nm), those effects became significant and began to affect the MOSFET threshold voltage and leakage currents in the "OFF-state." Extensive work has been done to explore the physics of the first two effects, and numerous device models have been developed to capture them in device and circuit simulations [14–17]. (Here, we will not give the details of those models. Readers with particular interests should refer to the related references.) In contrast to the quantum confinement and gate tunneling, quasi-ballistic transport and source-to-drain tunneling begin to significantly affect the device performance of the silicon MOSFET when the gate length scales down to 10 nm or less [18]. Therefore, the exploration of these mesoscopic transport effects is important for the description of silicon MOSFETs at their scaling limit, as well as the understanding of device physics of other nanoscale devices (to be discussed later). In the following paragraph, a simple description of the ballistic/quasi-ballistic transport [19–23] is presented, which gives us the upper performance limit of nanoscale transistors. Section 4.3 discusses the source-to-drain tunneling in silicon MOSFETs at the scaling limit.

In a conventional MOSFET, the channel length is much longer than the electron mean-free-path, so an electron will experience numerous collisions during its travel from the source to the drain. Nevertheless, when the channel length shrinks to less than the mean-free-path, an electron may go through the channel with no or little scattering, which is called ballistic/quasi-ballistic transport. According to the quasi-ballistic transport theory [2,22,23], the current under low drain bias can be written as (assuming nondegenerate statistics),

$$I_{DS} = \frac{\lambda}{L+\lambda} W Q_i(0) \frac{\upsilon_T}{2k_B T} V_{DS} \tag{4.1}$$

where λ is the electron mean-free-path, L is the channel length of the MOSFET, $Q_i(0)$ is the sheet electron density at the beginning of the channel, $V_T \sqrt{2k_B T/\pi m^*}$ is the unidirectional thermal velocity of nondegenerate electrons, and other symbols have their common meanings. For a long channel device, $L >> \lambda$, so Equation 4.1 becomes

$$I_{DS} = W Q_i(0) \frac{\upsilon_T \lambda}{2k_B T} \frac{V_{DS}}{L} \tag{4.2}$$

Because the mobility for nondegenerate electrons can be defined as $\mu_0 = \upsilon_T \lambda / (2k_B T)$ [21], Equation 4.2 is simply the well-known classical device equation based on the drift-diffusion theory [11]. When $L << \lambda$, the current approaches its upper (ballistic) limit,

$$I_{DS} = I_{ballistic} = WQ_i(0)\frac{\upsilon_T}{2k_BT}V_{DS} \tag{4.3}$$

The point is that the conventional device equations are an approximation valid when $L >> \lambda$. As MOSFET channel lengths approach the nanoscale, the classical MOSFET equations must be modified to capture quasi-ballistic transport. It is important for both device simulation and the development of circuit models for nanotransistors.

4.3 Ultimate Limits of the Silicon MOSFET

As the gate lengths of Si MOSFETs continue to shrink, the two-dimensional (2D) electrostatics become increasingly important, which causes the well-known short-channel effects (SCEs). At the same time, for the MOSFET with a gate length < 10nm, the quantum mechanical tunneling from source to drain may also be significant. It will degrade the subthreshold slope and increase the leakage current in the OFF-state. According to our previous work [18], the ultimate scaling limit of Si MOSFETs is determined by both the semiclassical SCEs (i.e., DIBL, V_T roll-off) and the S/D tunneling.

In Wang and Lundstrom [18], S/D tunneling has been extensively examined using the nonequilibrium Green's function (NEGF) approach [24], a general and rigorous quantum model for nanoscale transistors. (The 2D quantum simulator for double-gate Si MOSFETs, nanoMOS-2.5, is available at http://nanohub.purdue.edu.) The main conclusions are summarized next:

1. For the well-designed devices (with very thin silicon body and oxide layers that provide good electrostatics), S/D tunneling sets an ultimate scaling limit that is well below 10 nm.
2. S/D tunneling dominates OFF-current in the devices at scaling limit, and it may play an important role in the ON-state of ballistic devices.
3. Due to S/D tunneling, the sub-threshold slope saturates at low temperature (see Figure 4.2). Therefore, the leakage current in the OFF-state may still be high even at low temperature.

We also found that for a double-gate MOSFET with a 1-nm-thick silicon body and 0.6-nm(equivalent)-thick oxide layers, S/D tunneling sets a scaling limit of L = 5 nm if we require that *the subthreshold swing*

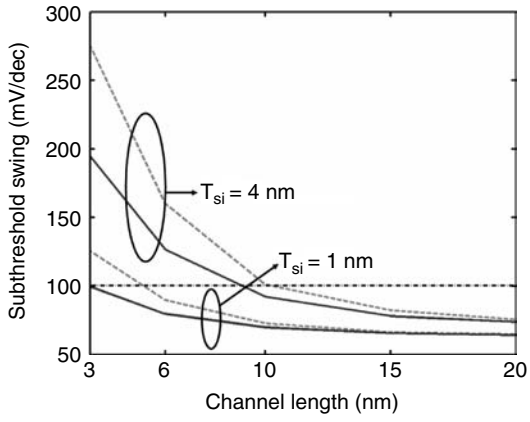

FIGURE 4.2 The subthreshold swing vs. temperature. The simulated device structure is a double-gate MOSFET with 0.6-nm(equivalent)-thick oxide layers. Two silicon body thicknesses (1 nm and 4 nm) are adopted in this simulation. The solid curves are for the semiclassical Boltzmann simulation (without S/D tunneling), while the dashed curves are for the quantum NEGF simulation (with S/D tunneling). (Obtained from J. Wang and M. Lundstrom, Does source-to-drain tunneling limit the ultimate scaling of MOSFETs? *IEEE Int. Electron. Devices Meeting (IEDM), Tech. Dig.*, pp. 707–710, San Francisco, CA, Dec. 2002. With permission.)

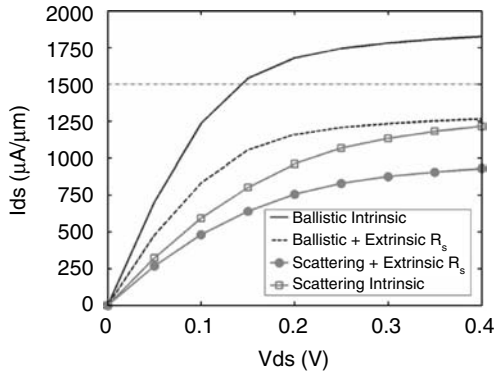

FIGURE 4.3 The top curve is the intrinsic ballistic current I^{i}_{ball}, and the dashed curve is I^{e}_{ball}, so the top two curves represent the ballistic intrinsic device. The bottom two are for intrinsic device with scattering. The curve with square markers represents I^{i}_{scatt}, and the fourth curve is I^{e}_{scatt}. (Obtained from S. Hasan, J. Wang, and M. Lundstrom, Device design and manufacturing issues for 10nm-scale MOSFETs: a computational study, *Solid State Electronics,* 48, 6, 867–875, 2004. With permission.)

is smaller than 100 mV/dec and the ON-OFF current ratio is larger than 100. Obviously, we could have different criteria to determine the ultimate scaling limit of a MOSFET. Likharev [25] proposed a criterion that the voltage gain of a CMOS inverter is larger than one, and used it to find a scaling limit of L = 2 nm. So two very important questions arise: How is the scaling limit of a MOSFET determined? What is the *worst* performance of a transistor that can be accepted by a very large scale integration (VLSI) circuit designer to build an IC chip? Clear answers to these questions require cooperation between device researchers and circuit engineers.

4.4 Practical Limits of the Silicon MOSFET

Section 4.3 discussed the ultimate scaling limit of a MOSFET. In practice, some technical issues (e.g., the source/drain series resistances, process variations, and power dissipation) may greatly affect device performance and set practical limits for MOSFETs.

In Hasan et al. [26], a computational study of the end-of-roadmap (L_G = 9nm) MOSFETs (high-performance) was presented. It was found that:

1. With a double-gate structure and a 3-nm-thick silicon body, the 10-nm-scale MOSFET can be realized but the ON-current is ~ 40% below the ITRS prediction. S/D series resistance and low gate overdrive ($V_{GS}-V_T$) were identified as limiting factors for the ON-current (see Figure 4.3 for details).
2. Process variations will seriously affect the device performance for the 10-nm-scale MOSFET. For example, a single monolayer (~ 0.3nm) variation in the silicon body thickness will cause more than 50% variation in the OFF-current (see Figure 4.4).

In summary, as the silicon MOSFET approaches its scaling limit, maintaining drive current at low supply voltages (~ 0.5V) will be very difficult, and device parasitics will be much more important than for current technology. Devices will be extremely sensitive to manufacturing variations. New design techniques will be needed to make use of devices with low drive current, high leakage, and large process variations.

4.5 Beyond the Silicon MOSFET

This section discusses several new types of FETs that are being explored by device physicists and engineers. Those devices could become either substitutes for the silicon MOSFET or complementary circuit elements that might be implemented into silicon IC circuits to improve their performance in the nanometer regime.

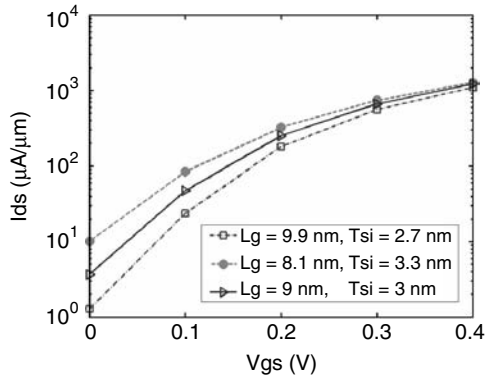

FIGURE 4.4 Intrinsic transfer characteristics of three different transistors. The top curve represents the worst transistor in terms of SCE, with L_G 10% smaller and t_{si} 10% larger, the middle one is the nominal device, and the bottom one represents the best device, with L_G 10% larger and t_{si} 10% smaller. (Obtained from S. Hasan, J. Wang, and M. Lundstrom, Device design and manufacturing issues for 10nm-scale MOSFETs: a computational study, *Solid State Electronics,* 48, 6, 867–875, 2004. With permission.)

4.5.1 Carbon Nanotube Transistors

One can think of a carbon nanotube as a 2D sheet of graphene (in which carbon atoms in a hexagonal lattice are bonded to three nearest neighbors as illustrated in Figure 4.5) that is rolled up into a tube. Depending on how the sheet is rolled up to produce a tube (in a "zigzag" pattern, "armchair," or in between (chiral), the nanotube can be either metallic or semiconducting). For semiconducting tubes, the bandgap is inversely proportional to the nanotube diameter. A diameter of 1 nm (a typical value) gives a bandgap of about 0.8 eV.

The interest in carbon nanotubes arises from the unique material properties they display. The one-dimensional (1D) energy band structure suppresses scattering, so ballistic transport can be achieved over relatively long distances. The thermal conductivity is exceptional, even higher than diamond, and nanotubes display excellent resistance to electromigration. These properties make nanotubes interesting for interconnects and heat removal in gigascale systems. Semiconducting nanotubes also display excellent transport properties, and the absence of dangling bonds may make it easier to incorporate high-K gate dielectrics into carbon nanotube field effect transistors (CNTFETs). Because the valence and conduction bands are mirror images of each other, n-type and p-type transistors should display essentially identical

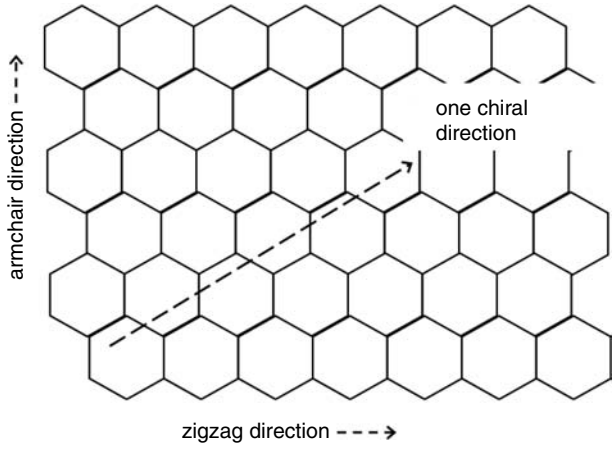

FIGURE 4.5 A 2D sheet of graphene showing the roll-up directions for different nanotubes.

characteristics, a significant advantage for complementary metal-oxide semiconductor (CMOS) circuits. Initially, CNTFETs suffered from high series resistance and low gate capacitance. Improved contacts are being developed, and new structures employ high-K gate dielectrics. The ITRS calls for an ON-current of 750 μA/μm (0.75 μA/nm) for PMOS transistors in 2016, which will be very difficult to meet by the silicon material at the low supply voltages needed ($V_{DD} \sim 0.5$ V). Experimental CNTFETs have already achieved over 7 μA/nm at 0.9 V [27].

It is clear that carbon nanotubes have great promise, but what are the challenges? The growth of CNTs with well-defined electronic properties is a critical issue. Growth from a catalytic seed can be used to control the CNT diameter, but it is more difficult to control the CNTs chirality (i.e., how it is rolled up). For applications in terascale systems, we will need to grow at least 10^{12} CNTs — all semiconducting with well-controlled diameters. Device structures and process flows are still primitive. One approach is to produce planar FETs with arrays of CNTs to provide sufficient current for conventional digital applications [28]. This approach aims to replace the silicon CMOS transistor with a higher-performance device. Another approach would be to explore the use of single nanotube electronics in dense locally interconnected architectures that could complement silicon CMOS. As CNT materials and device work proceeds, work at the system design level is needed to identify the most promising opportunities.

4.5.2 Organic Molecular Transistors

The organic molecular transistor is another possibility for post-CMOS devices. Figure 4.6 shows a schematic structure of the molecular FET. Compared with silicon MOSFETs and other nanotransistors, molecular FETs might have advantages on both fabrication and device performance.

1. The fabrication of molecular FETs could be with low cost, high controllability, and reproducibility. As we know, to fabricate a silicon MOSFET at the nanoscale, lithography and etching technology with extremely high resolution (< 10nm) is required, which may greatly increase the cost of IC fabrication. Moreover, the variations in lithography and etching can seriously affect the device performance. For CNTFETs (see previous paragraph), although the high-resolution lithography may not be needed for the device fabrication, the variations (i.e., the chirality and diameter of a CNT) from tube to tube could affect the controllability and reproducibility of the circuits. In contrast to silicon MOSFETs and CNTFETs, a molecular FET with numerous identical molecules might be realized at quite low cost by using the self-assembly technology [29]. The FET channel length is naturally equal to the length of the molecules so that the process variations would be effectively suppressed.
2. The molecular transistor has special physical properties that may be exploited to enhance the device performance. First, there could be no dopants in a molecular transistor. The type (n or p) of the FET can be determined by the gate work function [30]. As a result, the scattering inside the channel would be reduced. Considering the extremely short channel length of a molecular FET, transport inside the channel could be ballistic. Second, molecules are flexible and tunable,

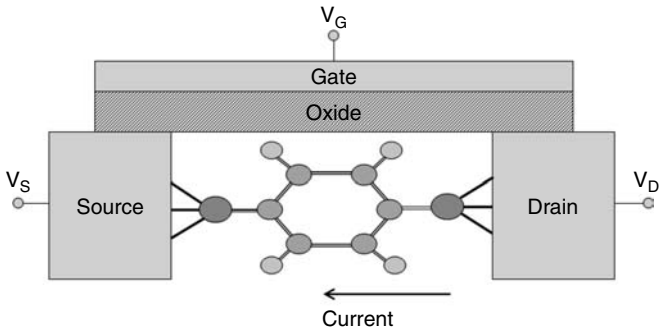

FIGURE 4.6 A schematic structure of the organic molecular transistor.

so it may be possible to control the molecules' shape (conformation) by a gate voltage [31]. This opens up the possibility of a molecular relay with a subthreshold swing better than the thermal-emission limit, $2.3k_BT/q$ (60 mV/dec at room temperature) [31]. Initial studies, however, show that thermal fluctuations of the flexible molecule are a serious issue [31].

As for any other nanotransistor, the organic molecular FET has its own challenges. Due to its extremely short channel, the molecular FET may seriously suffer the 2D electrostatics (so-called short channel effects, SCEs) (e.g., a 3-nm channel length may require a 0.2-nm equivalent oxide thickness to achieve good electrostatics, which is very difficult to realize in practice) [32]. The relatively low drive current may also limit its application as a logic circuit element. Therefore, the optimization of device performance becomes important for the future application of molecular transistors.

4.5.3 MOSFETs with New Channel Materials and Semiconductor Nanowire Transistors

A well-designed transistor should have an efficient gate control and good transport property (high channel mobility), so to improve the device performance of silicon MOSFETs, researchers are trying to exploit new channel materials and new gate geometry configurations.

Extensive experimental work [33–35] has been done on germanium and strained silicon, promising new channel materials that could provide higher mobility for both electrons and holes. On the other hand, silicon nanowire transistors are also being explored [6,36,37]. Such a 1D structure provides a possibility to make tri-gate or gate-all-around transistors that offer the best gate control. (Because the device physics of those transistors is similar to that of the silicon MOSFET, we do not discuss the details here.) With new channel materials or new gate geometry configurations, it may be possible to scale the MOSFET beyond the scaling limit of the planar silicon MOSFET.

4.6 Beyond the FET

Nanotechnology will not only provide the fabrication techniques to build nanoscale FETs, but also make it possible to realize some quantum-effects devices with special applications in the future electronics. Indeed, the most promising applications of molecular electronics may not be to replace Si MOSFETs but, instead, to complement CMOS with new capabilities. This section discusses two examples: the single electron transistor and the spin transistor.

4.6.1 Single-Electron Transistors

For future nanoscale transistors, the total number of electrons in the channel may be approximately 10, but a single-electron transistor (SET) is not just a smaller version of the same device. To produce a single electron transistor, the size of the "island" between the source and drain must be small enough so that the change in voltage due to a single electron is large compared to the thermal energy:

$$q^2/2C_G >> k_BT \tag{4.4}$$

Reliable room temperature operation requires an island size of less than about 1 nm, the size of a small molecule. In addition, we also require that the source and drain be weakly coupled to the gated island, which is usually accomplished by introducing tunnel barriers at the two contacts. When these conditions are met, some unique I-V characteristics result [38]. For example, the number of electrons on the island changes in discrete steps as the gate voltage increases, and a "Coulomb blockade" prevents current flow until V_{DS} exceeds a critical value. The critical voltage for conduction is periodic in gate voltage. Single electron transistors have been investigated for applications in digital systems, but they have several limitations [38]. The voltage gain is low and so is the drive current (because the tunnel junctions introduce a large series resistance). As might be expected, they are also extremely sensitive to

stray background charges. Certain hybrid SET/MOSFET circuits, however, combine single (or few) electron devices and CMOS transistors and have interesting possibilities for memory [38].

4.6.2 Spin Transistors

The operation of a conventional transistor is based on the charge that electrons carry, but electrons also carry spin, a fundamental unit of magnetic moment. The electron's spin is the basis for magnetic memories, but it is also conceivable that spin could be modulated by a gate to realize new types of devices [39]. For example, if the source and drain were ferromagnetic, then spin-polarized electrons might be injected into a semiconductor. If they retain their spin as they propagate across the channel, they could easily exit the ferromagnetic drain, but it may be possible to rotate the electron spins by a gate voltage thereby preventing them from exiting through the drain and contributing to the drain current.

Devices of this type have not yet been demonstrated, but current research is examining how to combine ferromagnetic metals and semiconductors, how to inject spin-polarized electrons into the semiconductor, and how to maintain the spin polarization once the electrons are in the semiconductor [40]. If devices of this type could be realized, they promise faster switching and lower switching energy than conventional electrostatic MOSFETs. Eventually, it may be possible to manipulate the spins of individual electrons (single electron spin transistors), which could lead to the realization of quantum computers.

4.7 From Microelectronics to Nanoelectronics

Nanoelectronics is not simply a smaller version of microelectronics; things change at the nanoscale. At the device level, silicon transistors may give way to new materials such as organic molecules or inorganic nanowires [41]. At the interconnect level, microelectronics uses long, fat wires, but nanoelectronics seeks to use short nanowires [41]. Fundamentally new architectures will be needed to make use of simple, locally connected structures that are imperfect and are comprised of devices whose performance varies widely.

We believe that 21st-century silicon technology has evolved into a true nanotechnology. Critical dimensions are already below 100 nm. The materials used in these silicon devices have properties that differ from the bulk. Nanoscale silicon transistors have higher leakage, lower drive current, and exhibit more variability from device to device. New circuits and architectures will need to be developed to accommodate such devices. It matters little whether the material is silicon or something else; the same issues face any nanoelectronics technology. It is likely that many of the advances and breakthroughs at the circuits and systems levels that will be needed to make nanoelectronics successful will come from the silicon design community.

Developing an understanding of how devices operate at the nanoscale is a good reason to support nanoscience research. Another reason is that devices to complement silicon technology might be discovered. For example, carbon nanotube FETs could be exquisite singlemolecule detectors, and SETs could be integrated with MOSFETs for high-density memory applications. Another possibility is molecular structures that improve the performance of a CMOS platform. For example, ballistic CNTs could be high performance interconnects and efficient at heat removal. Nanowire thermoelectric cooling could lower chip temperature and increase performance [42]. Therefore, research on nanoelectronics will prove to be a good investment for several reasons.

The successful development of nanoelectronics will require a partnership between science and engineering. It was the same for semiconductor technology. The scientific community developed the understanding of semiconductor materials and physics and the engineering community used this base to learn how to design devices, circuits, and systems. Figure 4.7 summarizes this partnership. Science works in the nanoworld with individual atoms, molecules, nanoscale structures and devices, and assembly processes. Systems engineers work in the macroworld on complex systems with terascale device densities. In the middle are the device and circuit engineers. They must learn to think and work at the nanoscale to build devices and circuits that can connect to the macroworld. Their job is to hide the complexity of

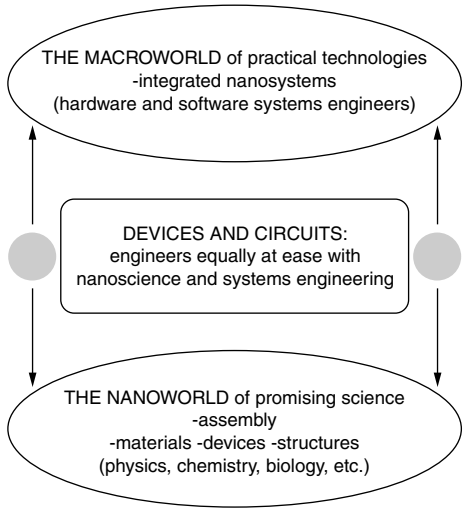

FIGURE 4.7 Science, engineering, and nanoelectronics.

the nanoscale device by packaging it in a form that systems engineers can use (e.g., a compact circuit model). To turn the promise of nanoscience into practical technologies, it is essential that the systems engineering community be engaged in the effort.

4.8 Conclusion

This chapter has introduced the emerging field of nanoelectronics — the new concepts and physical phenomena in the nanoscale MOSFET, the scaling limits of silicon MOSFETs, novel nanoscale FETs, quantum-effects devices with special applications, and the future of the electronics research. The scenario that we have outlined is an evolutionary one, but exponential evolution for another two to three decades would have a revolutionary impact on society. It is also true that it is hard to predict the future. Remember that the transistor was developed for a very specific purpose — to replace the vacuum tube; the integrated circuit was an unexpected bonus. The march of science and technology has carried us to the nanoscale; it is where the important questions are and where unforeseen breakthroughs may occur. Our march toward nanoelectronics is unstoppable. Who knows where it may lead.

4.9 Acknowledgments

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